The Historical Development of GaAs FET Digital IC Technology

PAUL GREILING, SENIOR MEMBER, IEEE

Abstract—**Only ten years have passed since the first GaAs field-effect transistor (FET) digital IC was reported showing the potential for gigabit data rates for microwave systems. During this short time, GaAs FET digital IC technology has matured to produce a 4K static RAM with 3-ns access time. This rapid progress of the technology is due in part of the synergistic research on FET's for microwave device applications, progress in materials growth, lithography, and processing techniques necessary to made uniform and reproducible devices and the support and leadership of the military services. The events that lead to the present, state of the art for GaAs digital IC technology are discussed in chronological order starting with Shockley's theory for the field effect transistor and concluding with performance projections for the technology. Discussions with individuals involved in the technology and review of the published literature have been taken into account in an attempt to outline the contributions that have been made to the technology.**

I. INTRODUCTION

AT FIRST GLANCE, the "marriage" of digital integrated circuits and microwave systems appears to be an "odd couple"; however, digital techniques are becoming increasingly more common in many microwave communication and radar systems. The improvements in signal-to-noise ratio, susceptibility to interference and real-time signal processing contribute to the conversion to digital microwave systems. Applications of this technology which are particularly attractive to the digital microwave system engineer are frequency synthesis, multiplexing and demultiplexing, counters, variable modulus dividers, shift registers, multipliers and memories. All of these circuits operate at clock frequencies well into the microwave range.

The emergence of solid-state devices fabricated in *III–V* compounds using micrometer or submicrometer lithography and having a maximum frequency of oscillation of tens of gigahertz, has produced integrated circuits for digital microwaves systems with gigabit data rates. The impact of this "blazing" speed on future digital systems has been the subject of many papers and talks, all of which promise significant performance improvements in high speed signal processing, high-speed computing, communications and measurement systems [1]–[13].

It is the purpose of this paper, as part of the IEEE MTT-S Centennial Issue, to highlight the events leading to the present state of the art in gigabit logic circuits. Such a review cannot possibly discuss every step leading to the present status of the technology, thus an apology is offered in advance to those whose contributions were not included. I have corresponded with many of the workers in the field who helped comprise the list of contributions that paved the way. This paper begins with the early work on the field-effect transistor (FET) and its evolution to a microwave device. At this point the technology divides into low noise devices and amplifiers, power devices and amplifiers, and digital IC's. The paper traces the major contributions to the GaAs digital IC technology. Competing technologies that offer potentially improved system performance are discussed for comparison. State-of-the-art performance for digital IC's operating at microwave frequencies is presented and projections of the technology are given.

Manuscript received January 11, 1984.
The author is with Hughes Research Laboratories, Malibu, CA 90265.

II. THE MICROWAVE FET

During the last decade, digital integrated circuits operating at microwave frequencies have utilized GaAs FET's. Only in the last few years have advanced Si nMOS and bipolar transistors attained the gain–bandwidth products necessary for gigahertz clock rate digital IC's. Therefore, this paper will focus on the evolution of GaAs FET's and IC's and will cite other competing technologies only for clarification or comparison.

The theory for the field effect transistor was developed by Shockley in 1952 [14]. The initial experimental work on FET's produced a much smaller field effect or current modulation than predicted and thus Bardeen proposed [14] that the surface states of the semiconductor trapped the added induced charge. Shockley proposed and analyzed in his 1952 classic paper, a p-n junction for the gate electrode, to eliminate the adverse effects of surface states. Shockley also noted the improved high-frequency performance of FET's compared with bipolar transistors due to the higher drift velocity of the majority carriers in the channel of the FET than of the minority carriers in the base of the bipolar transistor.

During the 1950's and into the 1960's, Si was the semiconductor universally used for FET's despite the lower mobility (speed) of the charged carriers. Other semiconductors, such as GaAs, were recognized as potentially having higher frequency of operation but because of the large density of surface states that pinned the Fermi level near the middle of the forbidden gap at the surface of the semiconductor and greatly reduced the field-effect modulation, they were not initially pursued. Only in Si could near ideal field-effect modulation be obtained due to chemical reactions of the surface which altered the surface state density.

0018-9480/84/0900-1144$01.00

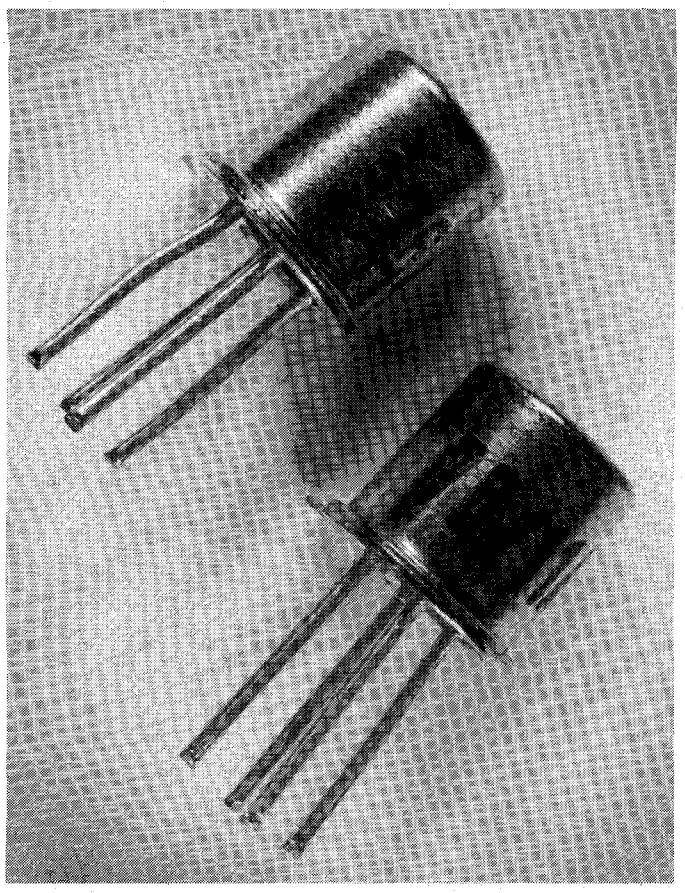


Fig. 1. Photograph of two of the original six GaAs FET's delivered on December 23, 1969, by Fairchild on Air Force Contract [18].

Professor C. A. Mead of California Institute of Technology (Cal Tech) pointed out that the Schottky-barrier depletion layer thickness was dependent on bias and independent of surface state density thereby making it ideal for the gate of FET's in those materials where MOS techniques were not possible [15]. Another high-frequency advantage of the Schottky barrier noted by Mead was that no charge storage effects exist as they do in p-n junctions. Professor Mead spent his Thanksgiving break from classes at Cal Tech. fabricating the first GaAs Schottky barrier FET in 1965 [16]. Though it was not designed for high-frequency performance, it did have a field-effect modulation as predicted by a surface state free theory. This was the first demonstration of the MESFET. In July 1967, Hooper and Lehrer of Fairchild reported the first microwave GaAs FET with an f_{max} of 3 GHz [17]. The device had a transconductance nearly 5 times that of a comparable Si device and a noise figure of 4 dB at 1 GHz. At this time, the Air Force initiated the development of the microwave GaAs MESFET with Fairchild. Two of the original six devices [18] that were delivered as part of the contract are shown in Fig. 1.

Several other research groups were also aware of the potential of GaAs FET's for microwave applications during this time. Zuleeg of McDonnell Douglas was pursuing the junction FET as originally proposed by Shockley under contract for the Air Force [19]. The gate of his junction

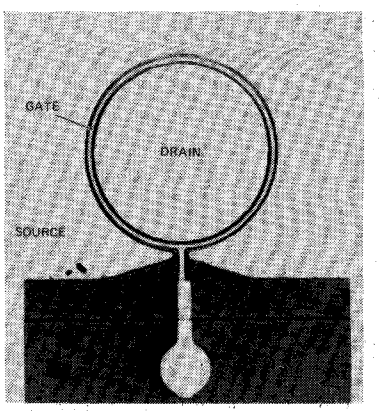


Fig. 2. Photomicrograph of IBM GaAs FET with 1-μm gate length [27].

FET was a zinc diffused p region in the n channel of the Si JFET's. The p-n junction gate circumvented the surface state problems. Zuleeg reported the first JFET in 1968 with a cutoff frequency of 2 GHz [20]. Workers at Siemens and Esaki and Dewitt of IBM were also interested in the potential of GaAs FET's [21]. However, the major IBM effort was headed by K. Drangeid at their Zurich laboratory. This work which was also sponsored by the Air Force, lead to the demonstration of the superior performance of GaAs MESFET's and gave the impetus for other research groups to start their own programs in this area. Initially Drangeid's group worked on Si MESFET's as a potentially higher frequency device than Si bipolar transistors [21], [22]. In the latter part of 1968, they reported a Si MESFET with an f_{max} of 12 GHz exceeding all of the bipolar results by 33 percent [23]. These results were subsequently extended to 15 GHz by early 1970 [21]. As noted by Wolf [24] and by Statz and Munch [25], the IBM group was aware of the improved performance offered by GaAs compared with Si. Their analyses predicted a factor of two improvement in f_{max} for GaAs MESFET's due to the higher drift velocity and mobility of electrons. However, the fabrication of the MESFET was nontrivial and several critical issues has to be addressed before its potential could be fully realized. Silicon was initially used because its properties and technology were much better established, though the extension to other, faster semiconductors was of prime interest [21]. On February 16, 1970, Wolf measured the power gain of a GaAs MESFET as a function of frequency up to 17 GHz [21]. The gain curve when extrapolated to 0-dB gain predicted an f_{max} of 30 GHz for Drangeid's GaAs MESFET, (Fig. 2), twice the frequency performance of their Si MESFET's. It was so much faster that, as Drangeid, Sommerhalder, and Walter observed in their paper reporting the accomplishment, "Devices have now been realized which are even too fast for presently available measuring equipment in this laboratory" [26]. For those of us associated with this technology, this measurement problem always seems to exist. We are in a "catch 22" situation in which we are developing circuit for instruments that are needed to measure the circuits we are developing. Continued analysis and optimization of the GaAs MESFET by Drangeid's group pushed the f_{max} of

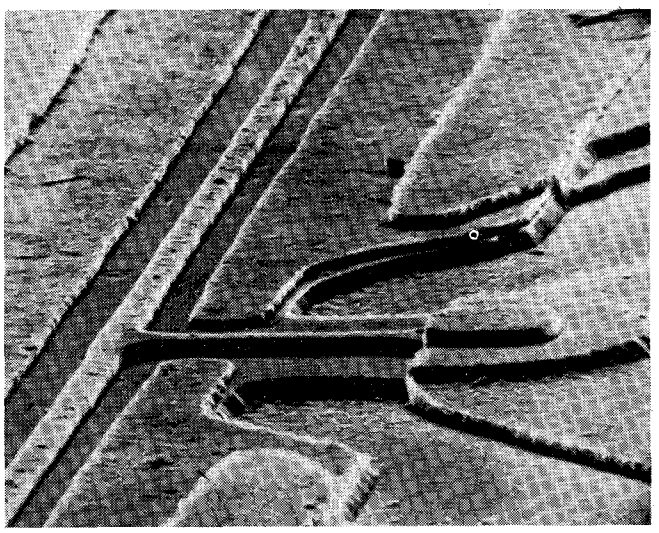


Fig. 3. SEM micrograph of the center section the HP low-noise microwave GaAs MESFET (1971) [29].

the device even higher, 50–60 GHz in January 1972 and 80–100 GHz in May 1973 for a 0.5-μm gate length GaAs MESFET [27], [28].

While Fairchild and IBM were making great strides in proving the potential of the GaAs MESFET as a microwave device, workers at HP were also developing their GaAs MESFET technology. At the 1972 ISSCC, Liechti *et al.* [29] reported a low-noise microwave GaAs MESFET (Fig. 3) with 3.5-dB noise figure at 10 GHz, unilateral power gain of 12 dB at 10 GHz and f_{max} of 40 GHz. These low noise results demonstrated the potential of the GaAs MESFET as a microwave device. By 1972 the impressive results reported by Fairchild, IBM, and now HP, demonstrating the superior performance of GaAs MESFET's, had convinced the microwave community, industry and government, to launch research programs in this area.

III. GaAs Materials Growth and Processing

The fabrication of GaAs MESFET's with microwave performance and incorporation in digital IC's required the solution to three critical technology problems: 1) high resistivity substrates for reduced parasitic capacitance and device isolation, 2) very thin and controlled doping density channels, and 3) extremely short gate lengths to insure high frequency performance. By no means were these the only issues, but represented three of the most important. The technology for growing semi-insulating substrates with resistivities greater than 10^6 $\Omega \cdot$cm was developed by Cronin and Haisty of TI with Air Force Support [30]. They were the first to demonstrate that semi-insulating GaAs crystals with room temperature resistivities of 10^8 $\Omega \cdot$cm could be pulled consistently by doping the melt with chromium.

Two of the most important methods in use today for producing semi-insulating GaAs are 1) Cr doped horizontal Bridgman (HB) and 2) liquid-encapsulated Czochralski (LEC) methods. The shortcomings of the HB method are that the crystals obtained are in the form of flattened cylinders with $\langle 111 \rangle$ axial orientation. The resulting $\langle 100 \rangle$ oriented slices are D-shaped. Also the chromium which must be added to ensure adequate compensation to produce high-resistivity GaAs, is thermally unstable which adversely affects device electrical uniformity [31]. Because of these problems, a great deal of effort has been expended to develop the direct synthesis LEC method, which eliminates the use of Cr as a dopant. Initially the LEC method was developed by Metz *et al.* for PdTe crystals and was applied to GaAs crystals by Mullin *et al.* [32], [33]. The first undoped, GaAs single crystals for use in ICs were produced by AuCoin of the Army Electronics Technology and Device Laboratory and by Swiggard *et al.* of the Naval Research Laboratory [34], [35]. The growth of high resistivity, semi-insulating GaAs for microwave device and circuit applications has been pioneered by Westinghouse Research Laboratories. Today, the LEC method appears to satisfy the requirements for high resistivity, thermally stable GaAs substrates.

The second critical technology issue, the very thin, controlled doping density active channel, was initially addressed by Hunsperger and Hirsch of Hughes [36]–[38]. They used ion implantation to form the active channel thus circumventing the variations in active layer thickness and doping density normally encountered for epitaxially grown layers. They reported standard deviations of the transconductance and pinchoff voltage of devices over a 1.5-cm diameter wafer of less than 8 and 9 percent, respectively. Successful demonstration and implementation of ion implantation for the fabrication of planar, GaAs IC's was due in a large part to Welch of Rockwell with DARPA support [39], [40]. The work of Welch provided a processing technology for 3-in wafers that produced the required channel, and thus device uniformity, necessary for LSI complexity circuits. Today, ion implantation is the standard procedure for forming the active channels of devices for IC's. Recently, Molecular Beam Epitaxy (MBE) has been introduced as a means to improve uniformity and reproducibility of the active layer. This growth technique for making very uniform semiconductor layers has been developed by Cho of Bell Laboratories among many others [41].

Finally, the third issue was that the small feature sizes required for high-frequency performance limited the gate lengths of GaAs MESFET's to no longer than 1 μm or even less. The initial results of IBM and HP were for 1 μm gate length devices. By reducing the gate length to 0.5 μm, IBM was able to achieve an f_{max} of 80–100 GHz. Silicon technologies are just now, a decade later, reducing their dimensions to micrometer and smaller values. In the early stages of the GaAs MESFET technology, contact photolithography was used to define 1 μm gates for discrete devices. The limit of optical lithography is approximately one micrometer and only very skilled operators could perform the alignments. Today optical projection lithography is used for IC's where yield is critical [40]. Electron-beam lithography was used by IBM to fabricate their 0.5-μm gate length GaAs MESFET's [28]. Later this lithography has been applied to digital IC's by Hughes [42].

TABLE I
EVOLUTION OF THE MICROWAVE FET

Date	Author	Ref.	Device	Device	Results
11/52	Shockley (IBM)	14	Theory for Junction FET		
7/64	Cronin and Haisty (TI)	30	High resistivity GaAs substrate growth	Cr doping	$> 10^8$ Ω-cm
11/65	Mead (Cal Tech)	15	GaAs MESFET	Channel:2.5 μm ρ =0.45 Ω-cm L_g= 10 μm	Low freqency I-V as predicted by theory
7/67	Hooper and Lehrer (Fairch.)	17	Microwave GaAs MESFET	Channel: 2 μm $N_D=2x10^{15}$ cm^{-3} W/Lg = 280	f_{max} = 3 GHz
5/68	Zuleeg (McDonnell Douglas)	20	Microwave GaAs JFET	Channel:2.5 μm $N_D=2x10^{15}$ cm^{-3} L_g = 5 μm	f_{max} = 2 GHz
1968	Drangied et al. (IBM)	21	Microwave Si MESFET		f_{max} = 12 GHz
2/70	Drangied et al. (IBM)	21	Microwave Si MESFET		f_{max} = 15 GHz
2/70	Drangied et al. (IBM)	26	Microwave GaAs MESFET	Channel:0.27 μm $N_D=10^{16}$ cm^{-3} L_g = 1 μm	f_{max} = 30 GHz
1/72	Baechtold et al. (IBM)	27	Microwave GaAs MESFET	Channel:0.15μm $N_D=10^{17}$ cm^{-3} L_g = 1 μm	f_{max} = 50-60 GHz
2/72	Liechti et al. (HP)	29	Microwave GaAs MESFET	Channel: 0.3μm $N_D=7x10^{16}$ cm^{-3} L_g = 0.9 μm	f_{max} = 40 GHz N.F. = 3.5 dB @ 10 GHz
5/73	Baechtold (IBM)	28	Microwave GaAs MESFET	Channel:0.15μm $N_D=10^{17}$ cm^{-3} L_g = 0.5 μm	f_{max} = 80-100 GHz
			Microwave Si MESFET	Channel:0.15μm $N_D=10^{17}$ cm^{-3} L_g = 0.5 μm	f_{max} = 22 GHz
12/73	Hunsperger and Hirsch (Hughes)	36	Ion Implanted Microwave GaAs MESFET	Channel:0.25μm $N_D=10^{17}$ cm^{-3} L_g = 2 μm	f_{max} = 20 GHz σg_m = 8% σV_p = 9%
9/73	Van Tuyl (IBM)	44	GaAs BFL gate	Channel:0.3μm $N_D=10^{17}$ cm^{-3} L_g = 1 μm	f_{max} = 15 GHz τ_g = 60 pS F.O. = 0 P_g = 90 mW

Today, optical projection lithography is used in LSI complexity circuits with 1.0-μm gate lengths and *e*-beam lithography to make submicrometer (i.e., 0.5 μm down to 0.2 μm) gate length devices. Other techniques such as X-ray, deep UV and focused ion beam lithography have achieved similar minimum feature sizes.

The important contributions to the early development of the FET up to the time of the first GaAs digital IC are summarized in Table I.

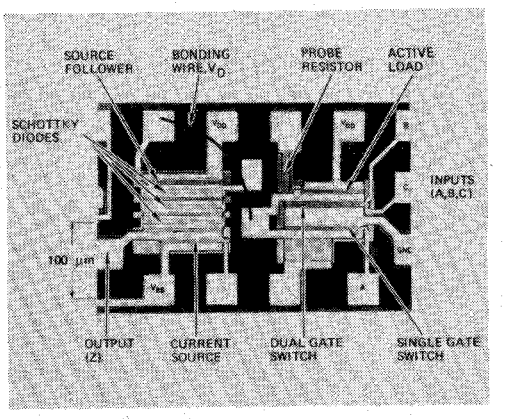


Fig. 4. Photomicrograph of the HP buffered FET logic gate [46].

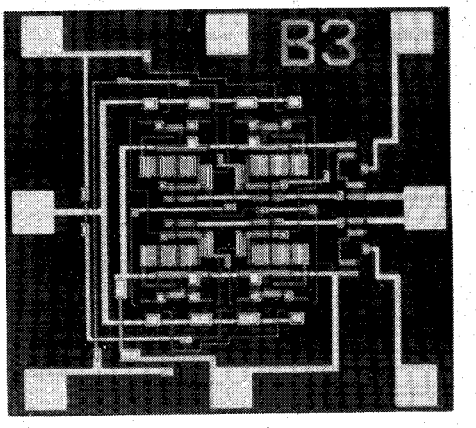


Fig. 5. Photomicrograph of the HP 4-GHz master-slave flip flop frequency divider [50].

IV. GaAs Digital IC's

During the early 1970's, the GaAs MESFET was being developed as a microwave device for low noise or power applications. The development of these technologies is discussed in a paper by McQuiddy *et al.* in this issue [43]. In 1972, the Air Force expanded their GaAs exploratory device program to include digital GaAs IC technology to meet the projected high data rate signal processing needs of the military [18]. The initial digital IC effort was with HP.

The concept for the basic buffered FET (BFL) logic gate and flip flop using GaAs MESFET's was conceived in July 1972 at HP [44]. (However, a similar logic gate design for a FET had been described by Csanky and Warner of Motorola in June 1963 [45].) The first year of the project was spent working on device problems which Van Tuyl called "Lag Effect," developing device computer models and fabricating and testing discrete devices. In August 1973, Van Tuyl measured the dc characteristics of the first GaAs BFL gate and on September 24, 1973, he obtained a 60-ps gate delay for a logic gate with a 1-μm gate length FET [32]. Based on these extremely promising results, Liechti directed the HP effort from a two prong approach of both low-noise FET's and digital IC's to primarily focus on the digital technology. At the 1974 ISSCC, Van Tuyl and Liechti reported their first of many GaAs logic circuits [46]. For the next few years, Liechti and Van Tuyl lead the

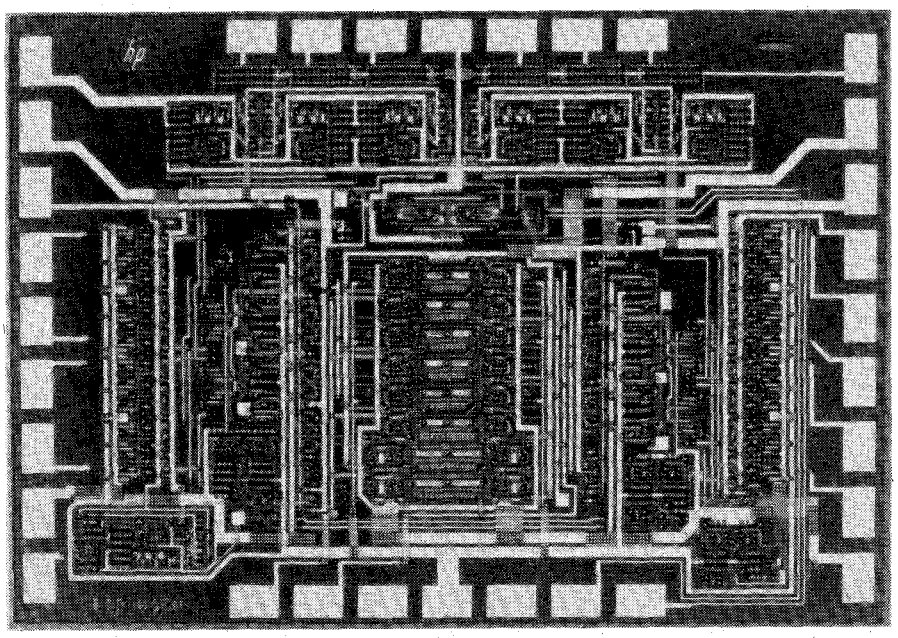


Fig. 6. Photomicrograph of the HP 5-Gbit/s data rate word generator [51].

development of the GaAs digital IC technology as other companies "jumped on the band wagon." Van Tuyl and Liechti gave numerous papers and talks based on their work [47]–[54]. C. Liechti, as the MTT-S National Lecturer in 1978–1979, drew standing room only audiences as more and more microwave system designers realized the significance of this technology. (As part of the arrangements for his lecture, Liechti always requested two complete projection setups, i.e., two projectors, two screens, two extension cords, etc. At the U.C.L.A. lecture, Tony Immorlica noted the backup equipment and questioned Charles if that is why HP used dual gate FET's in their logic circuits, the second gate acting as a backup.)

Several of the most significant contributions to the technology produced by the HP team were:

1) the first GaAs logic gate in 1974 (Fig. 4) [46],
2) the 4-GHz master-slave flip flop in 1976, (Fig. 5) [50],
3) the MSI, 5 Gb/s work generator in 1981 (Fig. 6) [51],
4) the universal laboratory test package with 14-GHz bandwidth (Fig. 7) [53].

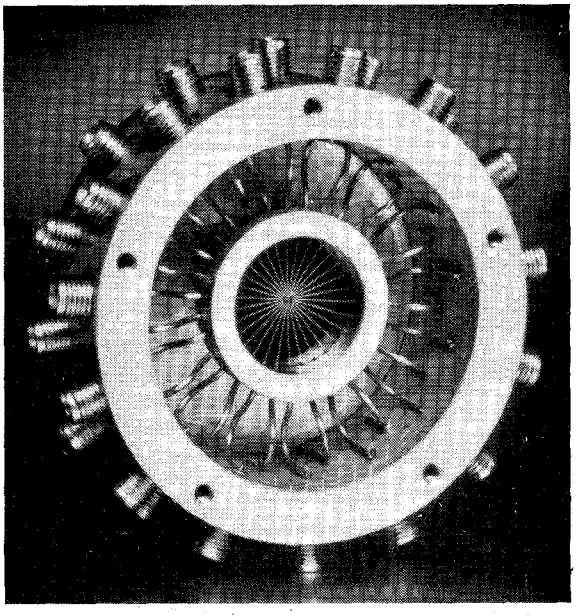


Fig. 7. Universal laboratory test package with 14-GHz bandwidth [53].

By the mid-1970's several more companies were starting to develop GaAs digital IC technology for their particular system needs. HP's effort was directed towards high-frequency instrumentation and not necessarily applicable to other system needs. Yoder of ONR in his keynote address at the 1979 MTT-S Symposium in Orlando, FL, told system houses that they must develop their own GaAs digital IC technology if they hoped to take full advantage of its potential [55].

In the latter part of the 1970's, Rockwell Science Center supported by DARPA, had a GaAs IC program in which an LSI complexity (>1000 gates) circuit was to be demonstrated. In order to stay within the power constraints (<2 W/chip) and still maintain high speed (100–200 ps/gate), Eden developed the Schottky diode FET logic (SDFL) gate which dissipated only one-fifth the power of the BFL gate used by HP while only doubling the gate delay [56], [57]. By the 1980 GaAs IC Symposium, Rockwell had successfully fabricated an 8×8 multiplier (Fig. 8) with 1008 SDFL gates [58]. This one circuit, designed by Eden *et al.* and fabricated by Welch *et al.* is a major milestone in the development of GaAs digital IC technology. Eden's flair for presenting interesting, informative and exciting technical talks and papers, interspersed with several "Gee Whiz" examples, helped convince microwave system engineers of the potential offered for improved performance by GaAs

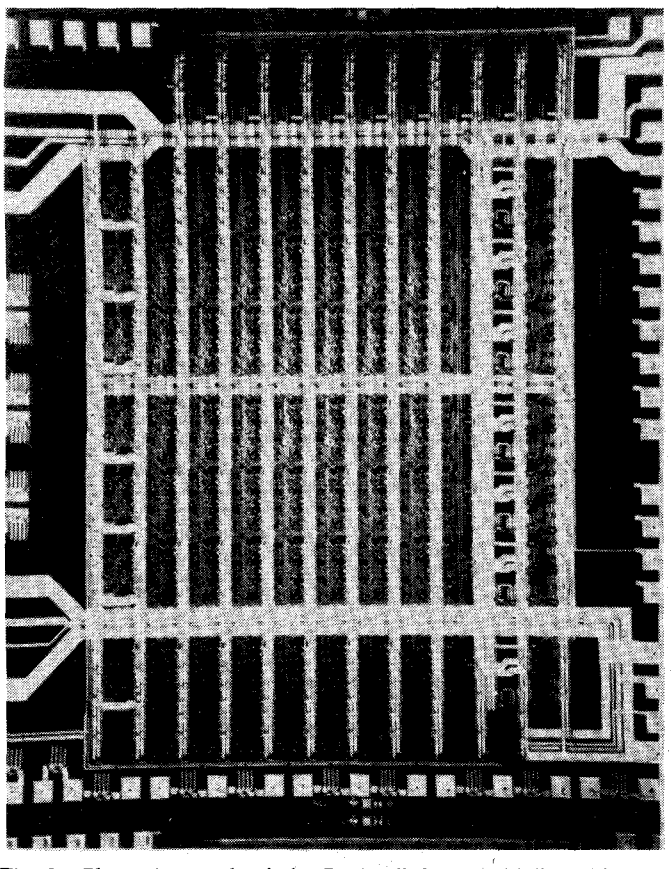


Fig. 8. Photomicrograph of the Rockwell 8×8 multiplier with 1008 gates.

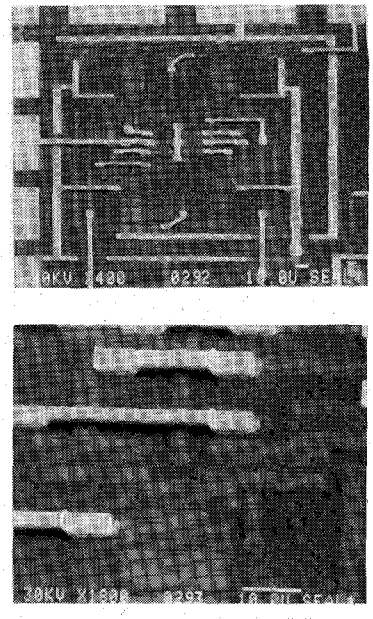


Fig. 9. SEM micrography of Hughes GaAs flip flop frequency divider with 0.5-μm gate length FET's [67].

digital IC's [59]–[64]. Welch's intuitive ability for processing, i.e., the early work on developing ion implantation and a planar GaAs IC process to the vertically integrated, 3-in wafer processing for high yield, LSI circuits, set the standard for the GaAs IC technology.

Other companies during the late 1970's were also developing their own technology to meet both company and government system needs. Hughes pursued two high-speed digital IC applications; 1) very high speed SSI to MSI circuits utilizing submicrometer gate length devices, and 2) very low power circuits utilizing enhancement-mode FET's. The high speed circuits sponsored by the Air Force used *e*-beam lithography to define the submicrometer gates. In 1978, 33-ps gate delay was obtained for ring oscillators and subsequently a 4 GHz and a 5.77 GHz (Fig. 9) divider circuits were reported [65]–[67]. The low-power circuits required development of enhancement-mode FET's (EFET). With Army support, Lundgren and Pierson developed the first U.S. EFET integrated circuits with deeply recessed gates [68], [69]. Because of the nonreproducibility of etching the channel under the gate as was required for the EFET, a planar self-aligned gate technology was developed at Hughes in which the EFET channel parameters are defined by ion implantation. The work was sponsored initially by the Air Force and subsequently by the Army and Navy. Gate delays as low as 25 ps with 3.1 mW/gate power dissipation were reported [70]. These results were improved to 15 ps, representing the fastest, all GaAs, room temperature logic gate [71].

Zuleeg at McDonnell Douglas has been developing JFET technology for a low-power, reproducible, and radiation hard device to be used in the design of high-speed logic and memories [72]–[75]. Zuleeg reported the first enhancement-mode JFET in 1975 [76]. By 1977, he had designed his first memory cell [19] and today on his DARPA sponsored program, he has fabricated a 256-bit static RAM with 5-ns access time and 100 nW/memory cell (Fig. 10) [19]. The latest SRAM circuit is designed with the first GaAs complementary logic, i.e., both n and p channel JFET's [77]. Zuleeg has performed extensive radiation testing of GaAs JFET IC's [75], [78], [79] and has shown that they are more radiation tolerant than any Si IC's, one potentially very important performance advantage of GaAs IC's.

TI has a GaAs digital IC effort to develop logic memory circuits. Also TRW is developing GaAs logic circuits and A/D converters sponsored by the Air Force. Honeywell and Tektronix started their GaAs digital technology programs later than many others but they have made tremendous advancements in a very short time. Tektronix has reported a 1200 cell gate array circuit that incorporates EFET's with reasonable yields and an 8-bit multiplexer/demultiplexer [80], [81]. Honeywell has reported a 432-cell gate array [82].

Companies outside the U.S. have been developing their own GaAs digital IC technology. Nuzillat [83], [84] at Thomson CSF in France has developed the low-power FET logic (LPFL) gate, which is a realistic tradeoff between processing technology and circuit characteristics, i.e., speed–power performance, noise margin, etc. Fig. 11 shows their microsequencer chip that is a portion of their 4-bit slice microprocessor with 250-MHz clock frequency which

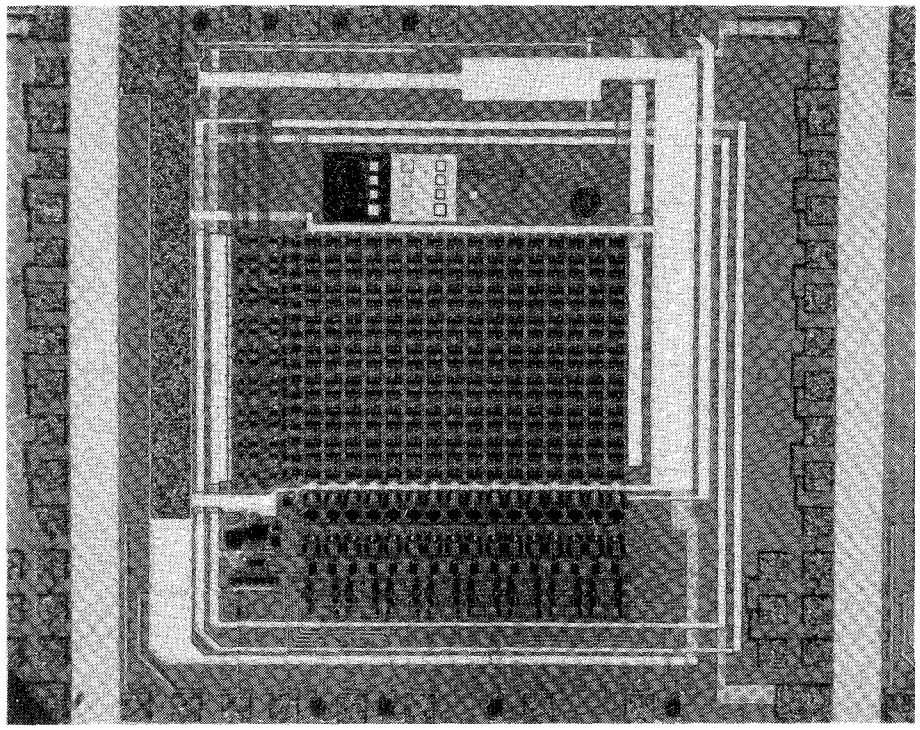


Fig. 10. Photomicrograph of McDonnell-Douglas 256-bit static RAM with complementary GaAs ENFET logic [77].

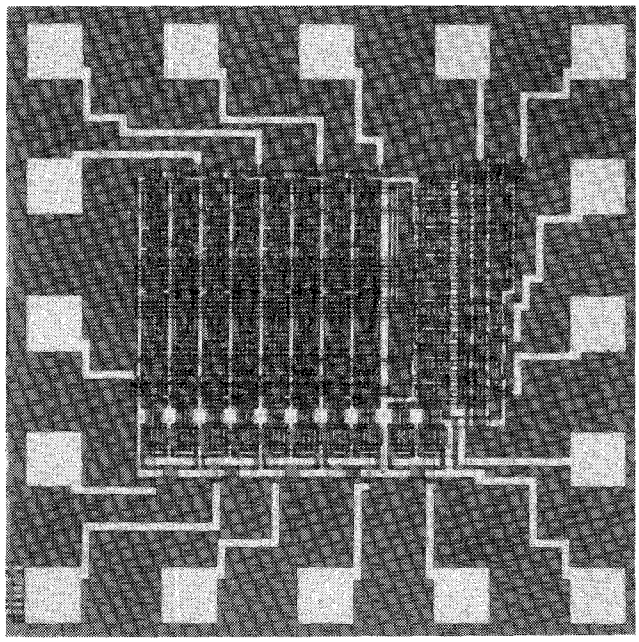


Fig. 11. Photomicrograph of Thomson-CSF microsequencer chip which is part of their 4-bit slice microprocessor with 250-MHz clock frequency.

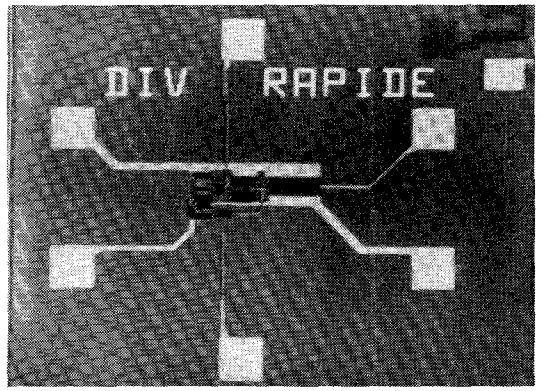


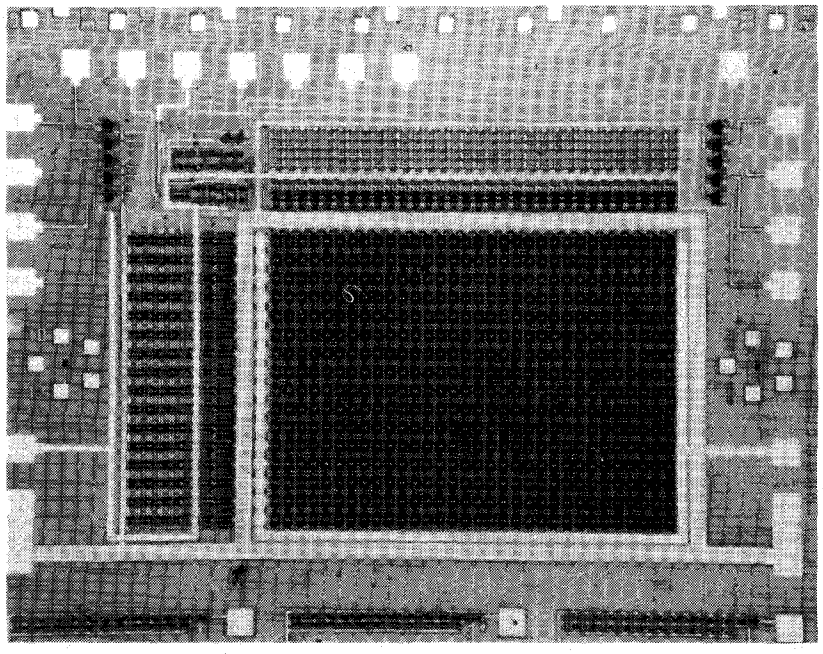
Fig. 12. Photomicrograph of LEP 10-GHz dynamic flip flop.

is now under development. Rocchi [85], [86] of LEP in France incorporated dynamic logic gates (Fig. 12) to achieve the fastest divider circuit reported, a 10-GHz divide-by-two circuit.

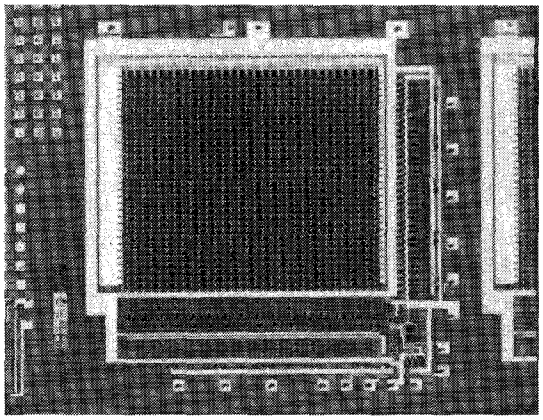
Certainly since the Rockwell 8×8 multiplier results, in 1980, several Japanese companies have mounted substantial GaAs IC development efforts at least partially in response to the fifth generation Computer Project. Companies such as Fujitsu, NTT, and NEC now play a leading role in the technology, One of the primary goals of the Japanese GaAs digital IC technology effort is a high-speed computer. To meet this goal, they have been developing the technology for memory circuits. They were the first to report

1) enhancement-mode MESFET circuits [87], [88],
2) self-aligned gate FET (SAGFET) [89],
3) sub 30 ps gate delays [90],
4) 1K SRAM (Fig. 13) [91],
5) 16×16 parallel multiplier (Fig. 14) [92],
6) 4K SRAM with 3-ns access time [93].

H. Ishikawa, M. Fukuta, K. Suyama, and N. Yokoyama of Fujitsu have emerged as leading practitioners of the



(a)



(b)

Fig. 13. Photomicrograph of (a) Fujitsu, and (b) Nippon Telegraph and Telephone 1K static RAM.

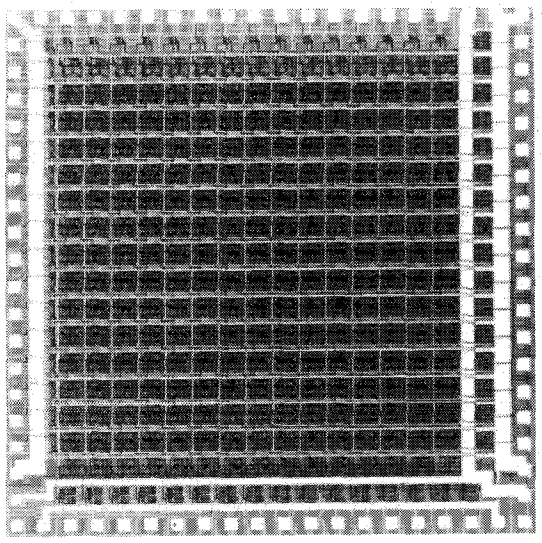


Fig. 14. Photomicrograph of Fujitsu 16×16 parallel multiplier.

technology based on their mastering of the self-aligned gate technology for digital IC's. M. Ino *et al.* of NTT are developing their own version of low-power enhancement-mode technology.

The growth of the technology can be measured in many ways. One convenient ways is to plot the complexity of circuits fabricated as a function of time as shown in Fig. 15 [6]. One must remember that the circuits shown in this figure represent initial laboratory test results which may or may not ever reach commercial viability. However, these circuits do show a rapidly maturing technology, due in part to the experience gained in fabricating even more complex Si IC's. A second, and probably more significant measure of the maturity of the technology, is that companies are now providing commercial circuits. DARPA has funded a GaAs IC foundry with a Rockwell/Honeywell team. Honeywell, Tektronix, and Harris are all advertising GaAs IC's and the only product of Gigabit Logic, founded by

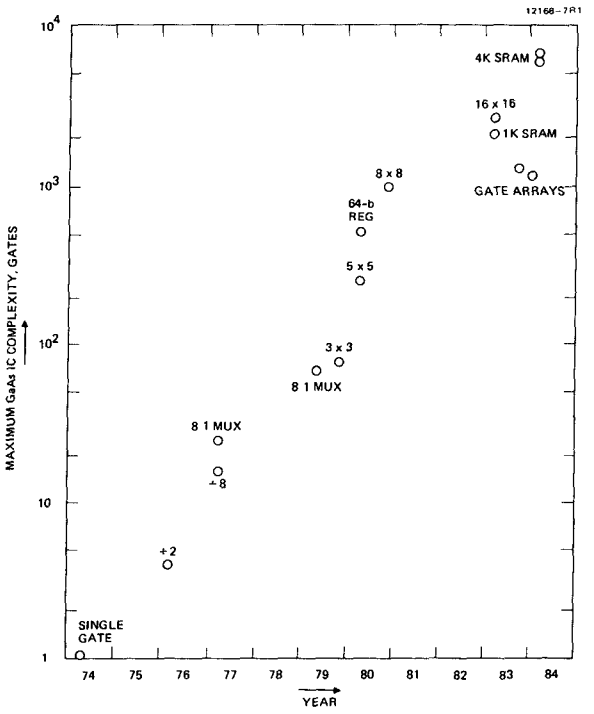


Fig. 15. Evolution of GaAs IC's complexity from origin to present (extension of original graph by Nuzillat *et al.*) [6].

several of the original Rockwell team, Blum, Eden, and Welch, will be GaAs devices and IC's.

V. Competing Digital IC Technologies

GaAs digital IC's must perform better than other rival technologies such as Si nMOS, Si bipolar, and newer and more exotic devices, if it is to survive over the long term. One of the important results of the high speed GaAs digital IC technology effort has been the impetus that it has provided to push Si IC's to higher frequencies. Lepselter *et al.* [94] at Bell Laboratories have fabricated nMOS circuits with X-ray lithography and achieved less than 30 ps gate delays and a 4K SRAM with 5-ns access time [95]. Silicon technology has an advantage over GaAs technology in that it is better understood and therefore more reliable and reproducible. Based on these extremely impressive results in Si nMOS, several strong exchanges in the press have been made as to "who is going to blow whom out of the water."

Bipolar IC's are another Si IC technology that is quietly and steadily improving its high-frequency performance. The Japanese have reported divider circuits that operate at 5.5 GHz with power levels comparable to GaAs IC's [96]. Others are also rapidly improving their performance in this area [97].

For a short time in the mid-1970's, a second GaAs technology, transferred electron logic devices (TELD) was a strong contender. This work was initially reported by Mause *et al.* [98], Sugeta *et al.* and Hartnagel [98]–[100]. Upadhyayula of RCA and Claxton of TRW carried out programs in this area for the Navy and Air Force [101]–[103]. Claxton reported a 10-GHz divider [104], a 1.4-Gbit/s data rate modulator and a 1.6-Gbit/s data rate demodulator, all designed with TELD's [102]. For his contributions to this technology, Claxton received the Microwave Application Award in 1979 [105]. Due to the dependence of the threshold of the device on material parameters, the reproducibility of devices in this technology was much more difficult than for FET's. This was truly a device before its time.

Another potential logic device is the permeable base transistor (PBT) being developed by MIT Lincoln Laboratory in both Si and GaAs [106], [107]. Snyder and Kubena of Hughes with support from Naval Ocean Systems Center (NOSC) analyzed the potential of the PBT as a logic device and concluded that the device had very poor drive capability which would significantly degrade performance in any IC of reasonable complexity [108]. Also, the difficulty of the fabrication technology may exclude this device from possible high-speed logic IC's of any reasonable complexity.

Two very promising devices which have emerged as a result of new epitaxial growth techniques, molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) are 1) the high electron mobility transistor (HEMT) [109], (so named by Fujitsu) (also known as the two-dimensional electron gas FET (TEGFET) named by Thomson CSF [110] or the selectively doped heterojunction transistor (SDHT), named by Bell Laboratories [111]), and 2) the heterojunction bipolar transistor (HJBT) [112], [113]. Fujitsu first announced HEMT device results in May 1980 and they predicted 3 to 10 times improvement in the high-frequency performance over the GaAs MESFET at 77K [109]. Their device design was based on the original work on mobility enhancement in heterojunction structures by Dingle *et al.* in 1978 [114]. Since Fujitsu's initial HEMT results in 1980, they have reported:

1) devices with transconductance over 400 mS/mm [115],
2) 16.8-ps gate delay at room temperature [115],
3) 12.7-ps gate delay at 77K [115]
4) 8.9-GHz divide-by-two circuit at 77K [116].

They are presently fabricating and testing a 1K SRAM [117]. Rockwell has recently achieved 12.2-ps gate delay at 77K with their HEMT circuits [118]. The rapid advance of this technology has been due in part to its similarity to GaAs digital IC technology. The key issue in HEMT technology is the MBE growth of thin layers of AlGaAs and GaAs. Because of its similarities to GaAs IC's, and its potential speed and power performance payoff, HEMT technology is a strong contender with GaAs MESFETs.

The HJBT is being developed at both TI and Rockwell. The advantage of the HJBT was first pointed out in 1957 by Kroemer [112]. During the early 1960's there were efforts to develop GaAs bipolar transistors as high speed, high-temperature devices. These efforts met with disappointing results because of material and process problems and were terminated in the late 1960's. After successful applications of GaAs MESFET's for microwave and digital

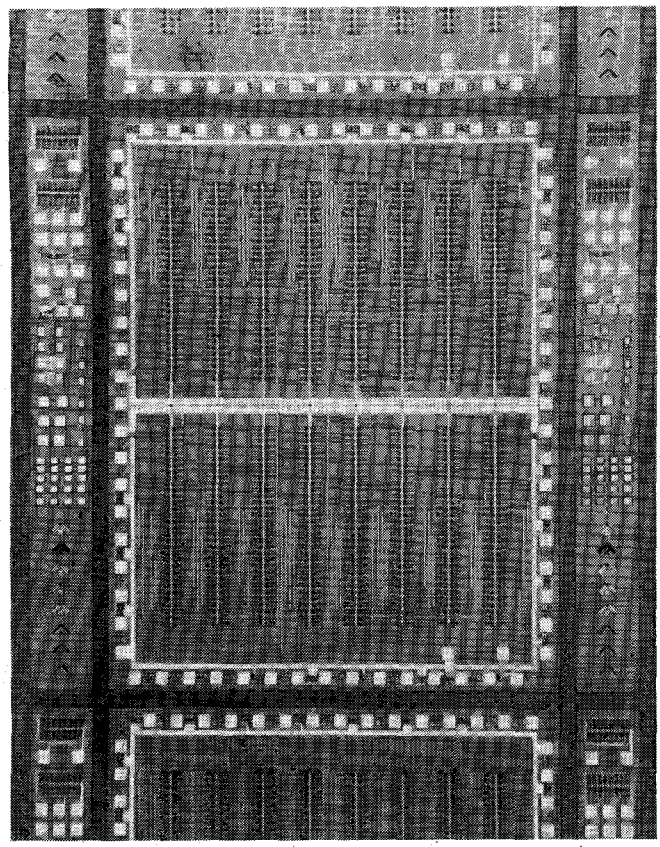


Fig. 16. Photomicrograph of TI 1K I^2L gate array with AlGaAs/GaAs HJBT's [121].

applications, Yuan of TI reexamined the potential for GaAs bipolar technology taking into account advances in materials and processing technology. TI fabricated the first ion implanted GaAs bipolar transistor in 1978 [119]. In 1980, TI fabricated the first inverted HJBT using MBE. Logic circuits have now been developed using these inverted transistors. This technology is now being applied to the development of gate arrays at TI with DARPA support using an I^2L circuit configuration [120]. The development of a 1K gate array will be reported at the 1984 ISSCC (Fig. 16) [121]. Asbeck *et al.* of Rockwell have been pursuing HJBT's in ECL circuits [122]. At the 1983 GaAs IC Symposium, Asbeck reported the first ECL HJBT circuits with 2-μm design rules yielded 185-ps gate delays [123]. Projections of 15-ps gate delays were made for improved device design. The HJBT technology is still very young and, therefore, it is difficult to make any predictions of its success.

VI. Summary

Digital IC technology operating at gigabit data rates will have a significant impact on the performance of digital microwave systems in the next decade. The technology that will be used, Si nMOS, Si bipolar, Si CMOS, GaAs MESFET, HEMT, HJBT, or some new device, will most likely depend on the application. Each technology has certain characteristics that make it the most appropriate technology for a given application, i.e., radiation tolerance, low temperature operation, ultra high speed, etc. Therefore, it is likely that the majority of these technologies will be available for the digital microwave system designer for a specific application. As the technology transfers from the research laboratory into the development and production environment, as is presently happening, the real test of the technology will be its ability to provide a significant performance advantage at a reasonable cost.

TABLE II
Projected Performance for Digital IC Technology

o	Gate loaded delay, $\leq$ 50 ps
o	Power dissipation $\leq$ 50 - 200 μW/gate
o	Complexity, MSI through VLSI
o	Preprocessor speed $\geq$ 5 GHz
o	A/D converter with $\geq$ 1 GS/s with 8-bit accuracy
o	Signal processor $\geq$ 1 GHz clock frequency
o	Memories: 4K SRAM with 1 ns access time 16K to 64K SRAM with 5 ns access time
o	Radiation tolerance of > 10^7 RADS, > 10^{10} RAD/s and > 10^{15} N/cm^2

The initial impact of the technology will be in preprocessors for signal processing in the front end of systems. As the technologies mature to LSI/VLSI complexity circuits, complete systems will be implemented on one or only several chips. A summary of projected performance for the digital IC technology is given in Table II. A factor of 2 to 10 times the system clock frequency over present systems is projected in the near future for signal processors and computers.

Acknowledgment

It must be mentioned that the development of any technology within the U.S., such as GaAs digital IC's, which is in a large part tied into microwave systems and applications for military use, is the result of visionary planning on the part of key government personnel. In this technology, the foresight of the Air Force, G. Rabanus, H. Steenbergen, and L. Micheel of the Avionics Laboratory at WPAFB who sponsored the early Fairchild and HP work and S. Roosild of Cambridge Labs who sponsored the IBM Zurich work,must be acknowledged. Also R. Reynolds and later S. Roosild of DARPA who sponsored the early ion implantation work at Rockwell and encouraged Rockwell to make the first LSI circuit should be noted.

The author wishes to express his thanks to those who contributed to this paper, Dr. Naoki Yokoyama of Fujitsu, Dr. Masayuki Ino of Nippon Telegraph and Telephone Public Corp., Dr. Gerard Nuzillat of Thomson CSF, Dr. Marc Rocchi of LEP, Dr. Charles Liechti and Dr. Fred Eisen of Rockwell Science Center, Rory Van Tuyl of HP, Dr. Rainer Zuleeg of McDonnell Douglas, Dr. William Wisseman of TI, Dr. Ken Sleger of NRL, Mr. Gordon Rabanus and Mr. Lutz Micheel of the Avionics Laboratory, WPAFB, and Dr. Charles Krumm and Dr. Robert Wilson of Hughes Research Laboratories.

REFERENCES

[1] C. A. Liechti, "Microwave field-effect transistors-1976," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 279–300, June 1976.

[2] R. C. Eden, "GaAs integrated circuits—technological overview," presented at the First Specialty Conf. on Gigabit Logic for Microwave Systems, Orlando, FL, May 3–4, 1979.

[3] B. G. Bosch, "Gigabit electronics review," *Proc. IEEE*, vol. 67, pp. 340–379, Mar. 1979.

[4] R. Van Tuyl and C. A. Liechti, "Gallium Arsenide spawns speed," *IEEE Spectrum*, pp. 41–47, Mar. 1977.

[5] A. D. Welbourne, "Gigabit logic, a review," *Proc. Inst. Elec. Eng.*, vol. 129, pt I, no. 5, pp. 157–172, Oct. 1982.

[6] G. Nuzillat, E. H. Perea, G. Bert, F. Danoy-Kavala, M. Gloanec, M. Peltier, T. Pham Ngu, and C. Arnado, "GaAs MESFET ICs for gigabit logic applications," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 569–584, June 1982.

[7] S. I. Long, B. M. Welch, R. Zucca, P. M. Asbeck, C. P. Lee, C. G. Kirkpatrick, F. S. Lee, G. R. Kaelin, and R. C. Eden, "High speed GaAs integrated circuits," *Proc. IEEE*, vol. 70, pp. 35–45, Jan. 1982.

[8] B. G. Bosch, "Device and circuit trends in gigabit logic," *Proc. Inst. Elec. Eng.*, vol. 127, pt. I, no. 5, pp. 254–265, Oct. 1980.

[9] P. T. Greiling, M. Waldner, R. E. Lundgren, D. E. Snyder, and R. G. Wilson, "Future applications for digital GaAs ICs," *LAMBDA*, vol. II, no. 1, pp. 44–47, First Quarter 1981.

[10] P. T. Greiling and M. Waldner, "Future applications and limitations for digital GaAs IC technology," *Microwave J.*, vol. 26, no. 2, pp. 74–87, Feb. 1983.

[11] R. C. Eden and B. M. Welch, "Ultra-high-speed GaAs VLSI approaches, potential and progress," in *VLSI Electronics-Microstructure Science*, New York: Academic, ch. 4, pp. 110–162, 1982.

[12] R. C. Eden, A. R. Livingston, and B. M. Welch, "Solid state integrated circuits: The case for gallium arsenide," *IEEE Spectrum*, vol. 20, pp. 30–37, Dec. 1983.

[13] P. T. Greiling, R. E. Lundgren, C. F. Krumm, and R. F. Lohr, Jr., "Why design logic with GaAs—and how?" *Microwave Systems News*, vol. 10, no. 1, pp. 48–60, Jan. 1980.

[14] W. Shockley, "A unipolar 'field-effect' transistor," *Proc. IRE*, vol. 40, pp. 1365–1376, Nov. 1952.

[15] C. A. Mead, "Schottky-barrier gate field effect transistors," *Proc. IEEE*, vol. 54, pp. 307–308, Feb. 1966.

[16] D. Howard Phillips of Aerospace Corp, Los Angeles, CA, private communication.

[17] W. W. Hooper and W. I. Lehrer, "An epitaxial GaAs field-effect transistor," *Proc. IEEE*, vol. 55, pp. 1237–1238, July 1967.

[18] Gordon Rabanus, Avionics Laboratory, WPAFB, Dayton, OH, private communication.

[19] R. Zuleeg, McDonnell Douglas Corp., Huntington Beach, CA, private communication.

[20] R. Zuleeg, "Epitaxial GaAs p-n junction field-effect transistors," *Proc. IEEE*, vol. 56, pp. 879–880, May 1968.

[21] M. B. Gusdansky, "The Schottky-barrier 'MESFET': A transistor with possibilities," *IBM Res. Rep.*, vol. 7, no. 1, 1971.

[22] K. Drangeid and R. Sommerhalder, "Dynamic performance of Schottky-barrier field-effect transistors," *IBM J. Res. Develop.*, vol. 14, no. 2, pp. 82–94, Mar. 1970.

[23] K. Drangeid, R. Jaggi, S. Middelhock, Th. Mohr, A. Moser, G. Sasso, R. Sommerhalder, and P. Wolf, "Microwave silicon Schottky-barrier field-effect transistor," *Electron. Lett.*, vol. 4, p. 326, 1968.

[24] P. Wolf, "Microwave properties of Schottky-barrier field-effect transistors," *IBM J. Res. Develop.*, vol. 14, no. 2, pp. 125–141, Mar. 1970.

[25] H. Statz and W. V. Munch, "Silicon and Gallium Arsenide field-effect transistors with Schottky-barrier gate," *Solid-State Electron.*, vol. 12, pp. 111–117, 1969.

[26] K. Drangeid, R. Sommerhalder, and W. Walter, "High speed Gallium-Arsenide Schottky-barrier field-effect transistors," *Electron. Lett.*, vol. 6, no. 3, pp. 228–229, Apr. 16, 1970.

[27] W. Baechtold, W. Walter, and P. Wolf, "X and Ku band GaAs MESFET," *Electron. Lett.*, vol. 8, no. 2, pp. 35–37, Jan. 1972.

[28] W. Baechtold, K. Daetwyler, T. Forster, T. O. Mohr, W. Walter, and P. Wolf, "Si and GaAs 0.5 m gate Schottky-barrier field-effect transistors," *Electron. Lett.*, vol. 9, no. 10, pp. 232–234, May 1973.

[29] C. Liechti, E. Gowen, and J. Cohen, "Microwave transistors, modulators and mixers," in *ISSCC Dig. Tech. Papers*, pp. 158–159, Feb 1972.

[30] G. R. Cronin and R. W. Haisty, "The preparation of semi-insulating Gallium Arsenide by chromium doping," *J. Electrochem. Soc.*, vol. 111, no. 7, pp. 874–877, July 1964.

[31] M. Umehara, "Trends in crystal growth technology for GaAs substrates," *JST News*, vol. 1, no. 6, pp. 9–12, Dec. 1982.

[32] E. Metz, *J. Appl. Phys.*, vol. 33, p. 2016, 1962.

[33] J. B. Mullin, B. W. Straughan, and W. S. Buckell, *J. Phys. Chem. Solids*, vol. 26, p. 782, 1965.

[34] T. R. AuCoin, R. L. Ross, M. J. Wade, and R. O. Savage, *Solid State Technol.*, vol. 2, p. 59, 1979.

[35] H. Lersoff and E. M. Swiggard, "Semi-insulating Gallium Arsenide substrates for integrated circuits: The state of the art," in *Dig. Abstracts, 1980 GaAs IC Symp.*, Las Vegas, NV, Nov. 1980.

[36] R. G. Hunsperger and N. Hirsch, "Field-effect transistors with implanted channels," *Electron. Lett.*, vol. 9, no. 25, pp. 577–578, Dec. 1973.

[37] R. G. Hunsperger and N. Hirsch, "Ion-implanted microwave field-effect transistors in GaAs," *Solid-State Electron.*, vol. 18, pp. 349–353, 1975.

[38] R. G. Hunsperger and N. Hirsch, "Ion implanted Gallium Arsenide semiconductor devices Fabricated in Semi-Insulating Gallium Arsenide substrates," U.S. Patent 3914784, Oct. 21, 1975.

[39] R. M. Welch and R. C. Eden, "Planar GaAs integrated circuits fabricated by ion implantation," in *Int. Electron Device Meeting Tech. Dig.*, pp. 205–208, Dec. 1977.

[40] B. M. Welch, Y. D. Shen, R. Zucca, R. C. Eden, and S. I. Long, "LSI processing technology for planar GaAs integrated circuits," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1116–1124, June 1980.

[41] A. Cho and C. Chen, "An $In_{0.53}Ga_{0.47}As$ very shallow junction gate structure grown by molecular beam epitaxy for field effect transistor applications," in *Dig. Papers Int. Electron Device Meeting*, pp. 96–99, Dec. 1981.

[42] "GaAs Schottky-gate FET integrated circuits," Contract F33615-76-C-1214.

[43] D. N. McQuiddy, Jr., J. W. Wassel, J. Bradner La Grange, and W. R. Wisseman, "Monolithic microwave integrated circuits. An historical perspective," *IEEE Trans. Microwave Theory Tech.*, this issue May 1984.

[44] Rory Van Tuyl, Hewlett Packard, Santa Rosa, CA, private communication.

[45] G. Csanky and R. M. Warner, "Put more snap in logic circuits with field-effect transistors," *Electronics*, pp. 43–45, June 1963.

[46] R. Van Tuyl and C. Liechti, "High speed integrated logic with GaAs MESFETs," in *Dig. Tech. Papers, ISSCC*, pp. 114–115, Feb. 1974.

[47] R. L. Van Tuyl and C. A. Liechti, "Gallium Arsenide digital integrated circuits," *Tech. Rep.* AFAL-TR-74-40, Air Force Avionics Lab., Contract F33615-73-C-1242, Mar. 1974.

[48] R. Van Tuyl and C. Liechti, "High speed GaAs MSI," in *Dig. Tech. Papers, ISSCC*, pp. 20–21, Feb. 1976.

[49] R. L. Van Tuyl and C. A. Liechti, "High-speed integrated logic with GaAs MESFETs," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 269–276, Oct. 1974.

[50] R. Van Tuyl, C. Liechti, R. Lee, and E. Gowen, "GaAs MESFET logic with 4 GHz clock rate," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 485–496, Oct. 1977.

[51] C. Liechti, G. Baldwin, E. Gowen, R. Jolly, M. Namjoo, and A. Podell, "A GaAs MSI word generator operating at 5 Gbits/s data rate," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 998–1006, July 1982.

[52] C. Liechti, C. Stolte, M. Namjoo, and R. Joby, "GaAs Schottky-gate field-effect transistor medium scale integration," *Tech. Rep.* AFWAJL-TR-81-1082, Air Force Avoinics Lab, Contract F33615-76-C-1342, Dec. 1982.

[53] C. Liechti, R. Joby, and M. Namjoo, "GaAs integrated circuits for error-rate measurement in high speed digital transmission systems," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 402–408, Aug. 1983.

[54] R. Van Tuyl, V. Kumar, D. D'Avanzo, T. Taylor, V. Peterson, D. Hornbuckle, R. Fisher, and D. Estreich, "A manufacturing process for analog and digital Gallium Arsenide integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 935–942, July 1982.

[55] M. Yoder, "Logic at microwave frequencies—courtship or marriage?" in *IEEE* 1979 MTT Symp., (*Orlando, FL*), *pp.* 7–10, *June* 1979.

[56] R. C. Eden, B. M. Welch, and R. Zucca, "Low power GaAs digital ICs using Schottky diode-FET logic," in *ISSCC Dig. Tech. Papers*, pp. 68–69, Feb. 1978.
[57] R. C. Eden, "Schottky diode FET logic integrated circuits," U.S. Patent 4300064, 1981.
[58] F. S. Lee, E. Shen, G. R. Kaelin, B. M. Walsh, R. C. Eden, and S. I. Long, "High speed LSI GaAs integrated circuits," presented at the 2nd GaAs IC Symp., Las Vegas, NV, Nov. 4–6, 1980.
[59] F. S. Lee, R. C. Eden, S. I. Long, B. M. Welch, and R. Zucca, "High-speed LSI GaAs integrated circuits," in *IEEE Int. Conf., Circuits and Computers*, (New York), pp. 697–700, 1980.
[60] R. C. Eden, "Comparison of GaAs device approaches for ultra-high-speed VLSI," *Proc. IEEE*, vol. 70, pp. 5–12, Jan. 1982.
[61] R. C. Eden, B. M. Welch, and R. Zucca, "Planar GaAs IC technology: Applications for digital LSI," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 419–426, 1978.
[62] S. I. Long, F. S. Lee, R. Zucca, B. M. Welch, and R. C. Eden, "MSI high speed low power GaAs ICs using Schottky diode FET logic," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 466–472, 1980.
[63] R. C. Eden, F. S. Lee, S. I. Long, B. M. Welch, and R. Zucca, "Multilevel logic gate implementation in GaAs ICs using Schottky diode-FET Logic," in *ISSCC Dig. Tech. Papers*, pp. 122–123; 265–266, Feb. 1980.
[64] R. C. Eden, "GaAs integrated circuits, MSI status and VLSI prospects," in *Int. Electron Devices Meeting Tech. Dig.*, pp. 6–11, Dec. 1978.
[65] P. T. Greiling, C. F. Krumm, F. S. Ozdemir, L. H. Hackett, and R. F. Lohr, Jr., "Electron-beam fabricated GaAs FET inverter," *IEEE Trans. Electron Devices*, vol. ED-25, p. 1340, Nov. 1978.
[66] P. T. Greiling, F. S. Ozdemir, C. F. Krumm, B. Sun, and R. F. Lohr, Jr., "Electron-beam fabricated GaAs integrated circuit," *Dig. Tech. Papers*, 1979 Int. Electron Devices Meeting, *pp.* 670–673, *Dec.* 1979.
[67] P. T. Greiling, R. E. Lee, R. S. Beaubien, R. P. Bryan, and M. Waldner, "Submicrometer GaAs Digital ICs," presented at the 1983 GaAs IC Symp., Phoenix, AZ, Oct. 1983.
[68] R. E. Lundgren, C. F. Krumm, and R. L. Pierson, "Fast enhancement-mode GaAs MESFET logic," *IEEE Trans. Electron Devices*, vol. ED-26, p. 1827, Nov. 1979.
[69] R. E. Lundgren, C. F. Krumm, and R. F. Lohr, Jr., "Enhancement-mode GaAs MESFET logic," Abstracts of IEEE Gallium Arsenide Integrated Circuit Symp., Lake Tahoe, NV, Sept. 1979.
[70] H. M. Levy, R. E. Lee, and R. A. Sadler, "A submicrometer self-aligned GaAs MESFET technology for digital integrated circuits," presented at the Device Research Conf., Boulder, CO, June 1982.
[71] R. A. Sadler and L. Eastman, "Self-aligned submicrometer ion-implanted GaAs MESFETs for high speed logic," presented at the Device Research Conference, Burlington, VT, June 1983.
[72] R. Zuleeg, J. K. Notthoff, and K. Lehovec, "Femotojoule high-speed planar GaAs E-JFET logic," *IEEE Trans. Electron Devices*, vol. ED-25, pp. 628–639, June 1978.
[73] J. K. Notthoff and C. H. Vogelsang, "Gate Design for DCFL with GaAs E-JFETs," Abstracts of IEEE Gallium Arsenide Integrated Circuit Symp., Lake Tahoe, NV, Sept. 1979.
[74] G. L. Troeger, A. F. Behle, P. E. Friebertshauser, K. L. Hu, and S. H. Watanabe, "Fully Ion Implanted Planar GaAs E-JFET Process," in *IEEE Int. Electron Devices Meeting Tech. Dig.*, (Washington, DC), pp. 497–500, Dec. 1979.
[75] R. Zuleeg, "Improved fast neutron tolerance of GaAs JFETs operation in the hot electron range," *IEEE Trans. Nuclear Sci.*, vol. NS-18, pp. 110–113, 1971.
[76] J. Notthoff and R. Zuleeg, "High speed, low power GaAs JFET integrated circuits," presented at the 1975 Int. Electron Device Meeting, Washington, DC, Dec. 1975.
[77] R. Zuleeg, J. Notthoff and G. Troeger, "Double-implanted GaAs complementary JFETs," to be published.
[78] R. Zuleeg and K. Lehovec, "Neutron degradation of ion-implanted and uniformly doped enhancement mode GaAs JFETs," *IEEE Trans. Nuclear Sci.*, vol. NS-25, pp. 1444–1449, Dec. 1978.
[79] G. L. Troeger and J. K. Notthoff, "A radiation-hard low-power GaAs static RAM using E-JFET DCFL," in *Dig.* 1983 GaAs IC Symp., *Oct.* 1983.
[80] A. Rode, T. Flegal, and George La Rue, "A high yield GaAs gate array technology and applications," *Dig.* 1983 GaAs IC Symp., *Oct.* 1983.
[81] G. McCormack, C. A. Rode, and E. Strid, "A GaAs MSI 8-bit multiplexer and demultiplexer," in *1982 GaAs IC Symp.*, (New Orleans, LA), Nov. 9–11, 1982.
[82] G. Lee, T. Steeves, M. Schroeder, R. Nelson, T. Vu, B. Hanzal, P. Roberts, M. Helix, S. Jamison, S. Hanka, and J. Brown, "A 432-cell SDFL GaAs gate array implementation of a four-bit slice event counter with programmable threshold and time stamp," *Dig. 1983 GaAs IC Symp.*, Oct. 1983.
[83] G. Nuzillat, G. Bert, F. Damay-Kavala, and C. Arnado, "High speed, low power logic ICs using quasi-normally-off GaAs MESFETs," *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 226–232, June 1981.
[84] G. Bert, Jean-Paul Morin, G. Nuzillat, and C. Arnodo, "High-speed GaAs static random-access memory," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 1014–1019, July 1982.
[85] M. Rocchi and D. Boccon-Gebod, "GaAs binary frequency dividers for high speed applications up to 10 GHz" *Electron. Lett.*, vol. 17, no. 4, pp. 168–169, Feb. 1981.
[86] M. Rocchi and B. Gabellard, "GaAs digital dynamic ICs for applications up to 10 GHz," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 369–376, June 1983.
[87] H. Ishikawa, H. Kusakawa, K. Suyama, and M. Fukuta, "Normally-off type GaAs MESFET for low power, high speed logic circuits," *ISSCC Dig. Tech. Papers*, pp. 200–201, Feb. 1977.
[88] T. Mizutani, M. Ida, and M. Ohmori, "An 80-ps normally-off GaAs MESFET logic," *Dig. IEEE/MTT-S First Specialty Conf. and Gigabit Logic for Microwave Systems*, pp. 93–101, 1979.
[89] N. Yokoyama, T. Mimura, M. Fukuta, and H. Ishikawa, "A self-aligned source/drain planar device for ultrahigh-speed GaAs MESFET VLSIs," *ISSCC Dig. Tech. Papers*, pp. 218–219, Feb. 1981.
[90] M. Ohmori, T. Mizutani and N. Kato, "Very low power gigabit logic circuits with enhancement-mode GaAs MESFETs," in *Dig. Paper 1981 IEEE-MTT Symp.*, pp. 188–190, (Los Angeles, CA), June 1981.
[91] N. Yokoyama, T. Ohnishi, H. Onodera, T. Shinoki, A. Shibatomi, and H. Ishikawa, "A GaAs 1K static RAM using tungsten–silicide gate self-alignment technology," in *ISSCC Dig. Tech. Papers*, pp. 44–45, Feb. 1983.
[92] Y. Nakayama, K. Suyama, H. Shimizu, N. Yokoyama, A. Shibatomi, and H. Ishikawa, "A GaAs 16×16 bit parallel multiplier using self-alignment technology," in *ISSCC Dig. Tech. Papers*, pp. 48–49, Feb. 1983.
[93] N. Yokoyama, H. Onodera, T. Shinoki, H. Ohnishi, H. Nishi, and A. Shibatomi, "A 3 NS GaAs 4K×1b static RAM," 1984 ISSCC, San Francisco, CA, Feb. 1984, to be presented.
[94] M. Lepselter, "Scaling the micrometer barrier with X-rays," presented at IEDM, Washington, DC, Dec. 1980.
[95] K. O'Connor and R. Kushner, "A 5 ns 4K×1 NMOS static RAM," in *ISSCC Dig. Tech. Papers*, pp. 104–105, Feb. 1983.
[96] T. Sakai *et al.*, "Gigabit logic bipolar technology: Advanced super self-aligned process technology," *Electronic Lett.*, vol. 19, pp. 283–284, Apr. 1983.
[97] Dr. Siegfried Knorr, Colby Instruments, Santa Monica, CA, private communication.
[98] K. Mause, A. Schlachetzki, B. Hesse, and H. Salow, "Monolithic integration of Gallium Arsenide-Gunn devices for digital circuits," in *Proc. Fourth Biennial Cornell Electrical Engineering Conf.*, 4:211—224, (Ithaca, NY), 1973.
[99] T. Sugeta, M. Tanimoto, T. Ikoma, and H. Yanai, "Characteristics and applications of a Schottky-barrier gate Gunn effect digitized-device," *IEEE Trans. Electron Devices*, vol. ED-21, pp. 504–515, Aug. 1974.
[100] H. Hartnagel, *Gunn-Effect Logic Devices*. New York: American Elsevier, 1973.
[101] L. C. Upadhyayula, R. E. Smith, and J. F. Wilhelm, "Transferred electron logic device (TELD) development," Ann. Rep., Contract N00014-75-C-0100, RCA Labs., Princeton, NJ.
[102] D. C. Claxton, T. D. Leisher, and T. G. Mills, "TED BPSK modulator/demodulator integrated circuit development," Final Tech. Rep., Contract N00014-76-C-0570, TRW Defense and Space Systems, Redondo Beach, CA, Feb. 1977.
[103] D. H. Claxton, T. G. Mills, and T. D. Leisher, "Transferred electron device design and circuits," Final Tech. Rep. Contract F33615-75-C-1219, TRW Defense and Space Systems, Redondo Beach, CA, Feb. 1977.
[104] D. H. Claxton, "TELD design for gigabit logic applications," presented at the First Specialty Conf. on Gigabit Logic for Microwave Systems, Orlando, FL, May 3–4, 1979.

[105] *Dig. Papers, 1979 IEEE MTT Symp.*, Orlando, FL, May 1979.
[106] C. O. Bozler and G. D. Alley, "Fabrication and numerical simulation of the permeable base transistor," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1128–1141, June 1980.
[107] C. Bozler, G. Alley, R. Murphy, D. Flanders, and W. Lindley, "Fabrication and microwave performance of the permeable base transistor," in *Dig. Papers IEEE Int. Electron Devices Meeting*, pp. 384–387, Dec. 1979.
[108] D. E. Snyder and R. Kubena, "Evaluation in the permeable base transistor for application in silicon integrated circuits," *Dig. Papers IEEE Int. Electron Device Meeting*, pp. 612–615, Dec. 1981.
[109] T. Mimura, S. Hiyamizu, T. Fujii and K. Nanbu, "A new field-effect transistor with selectively doped GaAs/$Al_xGa_{1-x}As$ heterojunctions," *Japanese J. Applied Physics*, vol. 19, no. 5, pp. L225–L227, May 1980.
[110] D. Delagebeaudeuf, P. Delescluse, P. Etienne, M. Lavinon, J. Chaplait, and Nuyen T. Linhs, "Two-dimensional electron Gas MESFET Structure," *Electron. Lett.*, vol. 16, no. 17, p. 667–668, Aug. 1980.
[111] J. DiLorenzo, R. Dingle, M. Fenci, A. Gossard, R. Hendel, J. Hwang, A. Kastalsky, V. Keramides, R. Kiehl, and P. O'Connor," Material and device considerations for selectively doped heterojunction transistors," in *Dig. Papers 1982 Int. Electron Device Meeting*, pp. 578–581, Dec. 1982.
[112] H. Kroemer, "Theory of a wide-gap emitter for transistors," *Proc. IRE*, vol. 45, pp. 1535–1537, Nov. 1957.
[113] H. Kroemer, "Heterostructure bipolar transistors and integrated circuits," *Proc. IEEE*, vol. 70, pp. 13–25, Jan. 1982.
[114] R. Dingle, H. L. Stromer, A. C. Gossard, and W. Wiegmann, "Electron mobilities in modulation-doped semiconductor heterojunction superlattices," *Appl. Phys. Lett.*, vol. 33, no. 7, pp. 665–667, Oct. 1978.
[115] M. T. Abe, N. Mimura, and H. Ishikawa, "New technology towards GaAs LSI/VLSI for computer applications," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 992–998, July 1982.
[116] K. Nishiiuchi, T. Mimura, S. Kuroda, S. Hizamiza, H. Nishi, and M. Abe, "Device characteristics of short channel high electron mobility transistor (HEMT)," presented at the Device Research Conf., Univ. of Vermont, Burlington, June 20–22, 1983.
[117] T. Mimura, K. Nishiuchi, M. Abe, A. Shibatomi, and M. Nobayashi, "High Electron Mobility Transistors for LSI Circuits," *Dig. Tech. Papers, 1983 Int. Electron Device Meeting*, pp. 99–102, Dec. 1983.
[118] C. P. Lee, D. Miller, D. Hou, and R. Anderson, "Ultra high speed integrated circuits using GaAs/GaAl As high Electron mobility transistors," presented at the Device Research Conf. Univ. of Vermont, Burlington, June 20–22, 1983.
[119] William Wisseman, Texas Instruments, Dallas, TX, private communication.
[120] H. T. Yuan, "GaAs Bipolar Gate Array Technology," in Digest of Papers for 1982 GaAs IC Symp., pp. 100–103, Nov. 1982.
[121] H. Yuan, W. McLevige, H. Shih, and A. Hearn, "GaAs heterojunction bipolar 1K gate array," to be presented at the 1984 ISSCC, San Francisco, CA, Feb. 1984.
[122] P. M. Asbeck, D. L. Miller, R. A. Milano, J. S. Harris, Jr., G. R. Kaelin and R. Zucca, "(Ga,Al) As/GaAs bipolar transistors for digital integrated circuits," in *Dig. 1981 IEDM*, pp. 629–632, Dec. 1981.
[123] P. M. Asbeck, D. L. Miller, R. J. Anderson, and F. H. Eisen, "Emitter-coupled logic circuits implemented with heterojunction bipolar transistors," in *Dig. 1983 GaAs IC Symp.*, pp. 170–173, Oct. 1983.

Paul T. Greiling (S'64–M'69–SM'82) was born in Cleveland, OH. He received the B.S.E.E. degree in 1963, and the B.S. degree in mathematics in 1963, the M.S.E.E. degree in 1964, and the Ph.D. degree in 1970 from the University of Michigan, Ann Arbor.

He joined the Faculty of Electrical Engineering at Northeastern University, Boston, MA, in 1970. While at Northeastern, he consulted for M.I.T., Lincoln Laboratory in the area of IMPATT diodes. In 1972, he joined the Faculty of Electrical Sciences and Engineering at the University of California, Los Angeles, where he did research on the theoretical analysis and experimental characterization of microwave solid-state devices. He consulted for local industry on millimeter-wave semiconductor devices. In 1976, he did research on GaAs FET's at Sandia Laboratory, Albuquerque, NM, as a Visiting Faculty Member. In 1976, he joined the staff at Hughes Research Laboratory, Malibu, CA, where he has been responsible for the design, modeling, and testing of GaAs FET IC's. At present, he is head of the GaAs IC Design and Analysis Section working on both photolithographic and electron-beam fabricated high-speed GaAs logic circuits.

Dr. Greiling is a member of MTT-S ADCOM, Eta Kappa Nu, Tau Beta Pi, and Sigma Xi.